Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit comprising:

an output circuit comprising plural output MOSFETs connected in parallel, said output MOSFETs connected in parallel being divided into plural groups and said plural groups being respectively divided into plural subgroups;

a first control means that, from among the plural output MOSFETs, selects the number of output MOSFETS to be turned ON to control output impedance; and forms selection signals;

a second control means that controls a slew rate by controlling a drive signal of the output MOSFETs that are turned ON and forms timing signals; and

plural output prebuffers each of which is coupled to each of said output MOSFETs;

~~wherein said first and second control means are capable of performing independently of each other.~~

wherein said plural output prebuffers receives each of said selection signals, said timing signals and data signals to be outputted and drives each of said plural output MOSFETs, and

wherein said first control means controls output impedance and said second control means controls a slew rate and wherein said first control means and said

second control means perform their respective control independently.

2. (Currently Amended) The semiconductor integrated circuit according to claim 1,

~~wherein the output MOSFETs connected in parallel are divided into plural groups,~~

~~the output MOSFETs of the plural groups are respectively divided into plural subgroups,~~

~~the first control means forms a signal for selecting the plural groups,~~

~~the second control means controls the timing of driving output MOSFETs of the plural subgroups, and~~

~~corresponding to data to be outputted, plural output MOSFETs comprising one or plural groups selected by the first control means are turned ON correspondingly to a drive timing formed by the second control means.~~

wherein one or plural groups selected by the first control means are turned ON correspondingly to said timing signals formed by the second control means.

3. (Previously Presented) The semiconductor integrated circuit according to claim 2,

output impedance controlled by the first control means is set so as to match a characteristic impedance of transmission lines through which signals conveyed by the output MOSFETs are transmitted.

4. (Currently Amended) The semiconductor integrated circuit according to claim 3, ~~wherein, corresponding to each of the output MOSFETs, an output prebuffer for driving each of the output MOSFETs is disposed, and~~ wherein thesaid output prebuffer is activated by the data ~~to be outputted~~ signals and asaid selection signal formed by the first control means, and wherein thea rise time of asaid drive signal conveyed to each of the output MOSFETs is changed by ~~a control~~ said timing signal formed by the second control means.

5. (Original) The semiconductor integrated circuit according to claim 4, wherein a resistance element is connected in series with each of the output MOSFETs.

6. (Previously Presented) The semiconductor integrated circuit according to claim 5, wherein a resistance value of the resistance element is almost equal to or greater than a resistance value of the ON-state output MOSFET.

7. (Original) The semiconductor integrated circuit according to claim 6, wherein the circuit is configured in which impedance ratios of output MOSFETs making up the subgroups are almost equal among the plural groups, to

prevent slew rate control from being influenced by a result of output impedance control.

8. (Original) The semiconductor integrated circuit according to claim 6,

wherein the output MOSFET comprises a first MOSFET of first conduction type that forms an output signal of a level corresponding to a power voltage side, and a second MOSFET of second conduction type that forms an output signal of a level corresponding to ground potential side of the circuit, and

the first MOSFET and the second MOSFET are respectively provided with the output prebuffers.

9. (Previously Presented) The semiconductor integrated circuit according to claim 8,

wherein the first MOSFET, the second MOSFET, and the resistance element are connected by one straight wiring to form a layout of a basic structure, and

two or more of the basic structures comprising the first MOSFET, the second MOSFET, and the resistance element are disposed in parallel in a stripe form in a direction orthogonal to the wiring.

10. (Original) The semiconductor integrated circuit according to claim 9,

wherein, in the plural layouts of the basic structures disposed in parallel, stripe units having lower impedance have larger MOSFET size in a direction of extension

of the wiring and smaller resistance size in a direction of extension of the wiring, while stripe units having higher impedance have smaller MOSFET size in a direction of extension of the wiring and larger resistance size in a direction of extension of the wiring, and the difference between the stripe units of the plural basic structures is made small.

11. (Previously Presented) The semiconductor integrated circuit according to claim 10, wherein the stripe units further include an antistatic diode connected correspondingly to the straight wirings.

12. (Currently Amended) The semiconductor integrated circuit according to claim 6,

wherein the first control means includes a resistance element connected to an external terminal, and forms ~~a~~said selection signal for selecting the MOSFETs so as to produce output impedance closest to a resistance value of the resistance element connected to the external terminal.

13. (Previously Presented) The semiconductor integrated circuit according to claim 12,

wherein the output circuit is divided into plural groups, which are interspersed on a semiconductor board,

the first control means is disposed on the semiconductor board,

the selection signal formed by the first control means is conveyed to a latch circuit disposed for each of the groups, and

the latch circuit captures the selection signal corresponding to a clock pulse, and conveys the captured selection signal to a corresponding output circuit.

14-27. (Canceled)